Review of Approximate Wallace-Tree Multiplier for VLSI Application

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***Abstract*— With the increasing demand for high-performance and energy-efficient VLSI systems, approximate computing has gained significant attention as a promising approach. This paper presents review of approximate wallace-tree multiplier for VLSI application. The Wallace-Tree multiplier is widely used multiplication architecture due to its reduced complexity and efficient utilization of resources. We explore recent research efforts that aim to leverage the concept of approximation within the Wallace-Tree multiplier to achieve better trade-offs between accuracy, power consumption, and area.**

Keywords—VLSI, Approximate, Wallace-Tree, Digital, Multiplier..

I. INTRODUCTION

The demand for high-performance and energy-efficient VLSI systems has been continuously growing with the advancement of modern technologies. Multiplication is a fundamental operation in digital systems, and designing efficient and accurate multipliers is crucial for various applications such as signal processing, image and video processing, machine learning, and cryptography. The Wallace-Tree multiplier has emerged as a popular choice due to its reduced complexity and efficient utilization of hardware resources [1].

The Wallace-Tree multiplier architecture is based on a combination of parallel multiplication and carry-save addition stages. It achieves higher performance by reducing the number of partial products and minimizing the carry propagation delay. This makes it particularly suitable for VLSI applications that require high-speed multiplication [2].

However, as the demand for even higher performance and lower power consumption continues to rise, researchers have turned their attention to approximate computing techniques as a means to achieve better trade-offs between accuracy, power consumption, and area. Approximate computing leverages the observation that many applications are tolerant to errors and can still produce acceptable outputs even with imprecise calculations. By introducing controlled approximations in the Wallace-Tree multiplier, it is possible to optimize the design for improved energy efficiency and reduced hardware complexity[3].

The concept of approximation within the Wallace-Tree multiplier involves relaxing the accuracy requirements of the multiplication operation. This can be achieved through various techniques, including reducing the operand bit-width, allowing for error-tolerant designs, applying probabilistic approaches, or employing weighted approximation schemes. These techniques introduce controlled errors or utilize statistical properties to achieve higher computational efficiency while maintaining an acceptable level of accuracy for the given application [4].

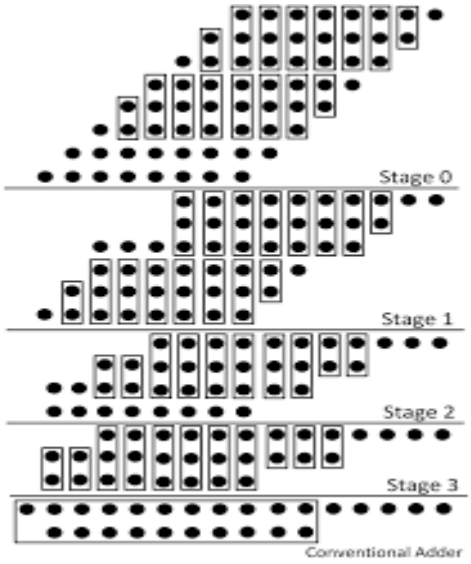

Figure 1: Approximate Wallace-Tree Multiplier

The design and implementation of approximate Wallace-Tree multipliers present a unique set of challenges and opportunities. Researchers and designers need to carefully balance the trade-offs between accuracy, power consumption, and area utilization. They must develop suitable approximation techniques, evaluation metrics, optimization algorithms, and design methodologies to explore the design space and identify the optimal configuration for a given application [5].

II. LITERATURE SURVEY

J. S, M et al.,[1] By using the Wallace Tree multipliers architecture and improving the adder in each Wallace Tree phase, reduce the unnecessary latency. The dominant logic

primitive was used for addition since it functions more effectively than NAND/NOR/IMPLY primitives. By executing several majority gates with in node columns, a high amount of circuit parallelism is utilized at the array level. These have an impact on the in-memory multiplier delay, which surpasses all other in-memory multipliers that have been previously reported. The proposed Majority Gates were developed in Verilog, modelled in Simulation 6.4c, and then synthesized using the Xilinx Tool

G. C. Ram et al.,[2] presented, a modified Wallace tree multiplier with several adders is presented. In every microprocessor and DSP circuit, the multiplier performs a vital function. The delay in multipliers is caused by the operating speed constraints of adders; by replacing standard adders with advanced adders in the multiplier's design, the total latency in the formation of partial products may be drastically decreased. In terms of memory and delay, the Wallace tree multiplier and the array multiplier are investigated. As wallace multiplier is preferable than array multiplier, the Wallace multiplier's construction is proposed utilizing Kogge Stone Adder (KSA) and carry select adder (CSLA) with Binary to Excess-l converter (BEC). The findings demonstrate that the suggested multiplier with BEC is effective, with minimal latency and memory use. The suggested wallace multiplier is implemented in Verilog and simulated in XILINX. The multiplier performance is validated using the Spartan 3E FPGA package. The designed multiplier is highly desirable for high-speedapplications.

D. OK et al.,[3] Convolutional Neural Networks (CNNs) have been effectively used for a variety of tasks, comprising image classification, detection and speech processing. CNNs possess computationally demanding methods and currently necessitates specialised hardware. Thus, hardware optimization for effective CNN accelerator design continues to be a difficult task. Most of the intensive computation on a CNN accelerator design is carried out by the processing element (PE). This article offers a novel processing element design based on Vedic multipliers and Wallace Tree adders as a substitute for hardware implementation. The proposed design achieves significant savings in hardware resources and power. The proposed Vedic multiplier results in minimum delay.

B. Thomas et al.,[4] Deep Neural Networks (DNNs) are useful for re-solving many practical problems such as traffic monitoring, vehicle detections. Among DNNs, Convolutional Neural Networks (CNNs) are generally used for image processing and video processing applications. In CNN, most of the computations are used up by convolution process. Winograd minimal filtering-based algorithm is one of the effective methods for computing convolution for small filter sizes. A prominant component of CNN accelerator design is the processing element (PE) unit which mainly comprises of the bulky multiply and accumulate (MAC) units and adder tree. It is the PE that performs the convolution operation. In this paper, new processing element has been designed using Modified Booth Encoding multiplier (MBE) and Wallace tree adders to reduce the amount of hardware resources and power consumption. This modified PE unit is implemented on an architecture known as UniWiG (Unified Winograd GEMM architecture). The proposed design reduces hardware complexity and achieves better power efficiency than the previous designs. Hardware realization of this work is done using Verilog Hardware Description Language(HDL) and tested on FPGA board.

S. Raveendran et al.,[5] Presented an inexact Baugh-Wooley Wallace tree multiplier with novel architecture for inexact 4:2 compressor optimised for realisation using reversible logic. The proposed inexact 4:2 compressor has ±1 Error Distance (ED) and 12.5% Error Rate (ER). The proposed multiplier is utilised in two applications 1) image processing - one level decomposition using rationalised db6 wavelet filter bank and image smoothing and 2) Convolutional Neural Networks (CNN). The efficacy of the proposed multiplier in image processing applications is estimated by measuring Structural Similarity Index Measure (SSIM) which is found to be 0.96 and 0.84 for image decomposition and smoothing respectively. In CNN based application, the efficiency is measured in scales of accuracy and is found to be 97.1%.

Y. d. Ykuntam et al.,[6] Major operation block in any processing unit is a multiplier. There are many multiplication algorithms are proposed, by using which multiplier structure can be designed. Among various multiplication algorithms, Wallace tree multiplication algorithm is beneficial in terms of speed of operation. With the advancement of technology, demand for circuits with high speed and low area is increasing. In order to improve the speed of Wallace tree multiplier without degrading its area parameter, a new structure of Wallace tree multiplier is proposed in this paper. In the proposed structure, the final addition stage of partial products is performed by parallel prefix adders (PPAs). In this paper, five Wallace tree multiplier structures are proposed using Kogge stone adder, Sklansky adder, Brent Kung adder, Ladner Fischer adder and Han carlson adder. All the multiplier structures are designed using Verilog HDL in Xilinix 13.2 design suite. The proposed structures are simulated using ISIM simulator and synthesized using XST synthesizer. The proposed designs are analyzed with respect to traditional multiplier design in terms of area (No. of LUTs) and delay (ns).

A. Sundhar et al.,[7] The major role of electronics device is to provide low power dissipation and compact area with high speed performance. Among the major modules in digital building blocks system, multiplier is the most complex one and main source of power dissipation. Approximate Computing to multiplier design plays major role in electronic applications, like multimedia by providing

fastest result even though it possesses low reliability. In this paper, a design approach of 16bit Wallace Tree approximate multiplier with 15-4 compressor is considered to provide more reliability. The 16×16 Wallace tree multiplier is synthesized and simulated using Xilinx ISE 14.5 software. The multiplier occupies about 15% of total coverage area. The dissipated power and delay of the multiplier are 0.042μw, 3.125ns respectively.

S. T. Bala et al.,[8] usage of additional circuits will finally result in increased area which in turn increases the power consumption also. To overcome these disadvantages, Approximate Wallace Tree Multiplier is implemented using incomplete adder cell (ICAC) and Accurate Compressor with Cin and Cout ignored (ACCI2) circuits. It is found out that it reduces the area compared to normal Wallace Tree Multiplier Design. Here, another method for Approximate Wallace multiplier using 4:2 compressors is proposed to keep the area overhead minimal. This method uses four to two compressors for addition and this circuit is used in the Approximate Wallace Tree Multiplier. The above designs are synthesized using Synopsys e and the power consumed and area occupied by both the methods is compared. By comparing, the multiplier with compressor minimizes the area by 98.39% when compared to Approximate Multiplier which also reduces the power consumption by 98.13%.

I. Qiqieh et al.,[9] presented an energy-efficient approximate multiplier design approach. Fundamental to this approach is configurable lossy logic compression, coupled with low-cost error mitigation. The logic compression is aimed at reducing the number of product rows using progressive bit significance, and thereby decreasing the number of reduction stages in Wallace-tree accumulation. This accounts for substantially lower number of logic counts and lengths of the critical paths at the cost of errors in lower significant bits. These errors are minimised through a parallel error detection logic and compensation vector. These gains are achieved at a low loss of accuracy, estimated at less than 0.0554 of mean relative error. To demonstrate the impact of approximation on a real application, a case study of image convolution filter was extensively investigated, which showed up to 62% (without error compensation) and 45% (with error compensation) energy savings when processing image with a multiplier using 4-bit logic compression.

R. B. S. Kesava et al.,[10] Multipliers are major blocks in the most of the digital and high performance systems such as Microprocessors, Signal processing Circuits, FIR filters etc. In the present scenario, Fast multipliers with less power consumption are leading with their performance. Wallace tree multiplier with carry select adder (CSLA) is one of the fastest multiplier but utilizes more area. To improve the performance of this multiplier, CSLA is replaced by binary excess-1 counter(BEC) which not only reduces the area at gate level but also reduces power consumption. Area and power calculations for the Wallace tree multiplier using CSLA with BEC are giving good results compared to regular Wallace tree multiplier

III. CHALLENGES

Followings are the challenges in approximate wallace-tree multiplier.

- The Accuracy-Reliability Trade-offs: One of the key challenges in designing approximate Wallace-Tree multipliers is finding the right balance between approximation and maintaining acceptable accuracy. Determining the level of approximation that still produces reliable results without compromising the overall functionality of the system is a complex task. The trade-off between accuracy and reliability needs to be carefully evaluated, considering the specific requirements of the target application.
- Validation and Verification Techniques: Verifying the correctness and performance of approximate multipliers poses significant challenges. Traditional validation and verification techniques may not be directly applicable due to the probabilistic nature of some approximation techniques or the non-deterministic effects of errors introduced. Developing specialized validation methodologies, including error modeling and simulation techniques, is essential to ensure the accuracy and reliability of the approximate multiplier designs.
- Real-Time Adaptation and Dynamic Approximation: Many VLSI systems require real-time adaptation and dynamic adjustment of their operation based on varying input data or changing environmental conditions. Incorporating dynamic adaptation mechanisms into approximate Wallace-Tree multipliers introduces additional challenges. Efficient techniques for dynamically adjusting the level of approximation or adapting to different error budgets in real-time scenarios need to be developed.
- Emerging Technologies and Approximate Computing: The emergence of new technologies, such as nanoscale devices or emerging non-volatile memories, presents both

opportunities and challenges for approximate computing. These technologies may have unique characteristics and constraints that need to be considered in the design of approximate Wallace-Tree multipliers. Exploring the synergy between approximate computing and emerging technologies can lead to novel design paradigms but also requires addressing new challenges in terms of design constraints, reliability, and energy efficiency.

- Energy-Accuracy Optimization: Power consumption is a critical consideration in VLSI design. While approximate computing techniques can reduce power consumption, achieving the optimal trade-off between energy efficiency and accuracy remains a challenge. Developing sophisticated optimization algorithms and design methodologies that can explore the multi-dimensional design space and identify the Pareto-optimal solutions for energy and accuracy trade-offs is a complex task.

- Integration and Compatibility: Approximate Wallace-Tree multipliers need to be seamlessly integrated into existing VLSI systems and architectures. Ensuring compatibility with standard interfaces, tools, and design flows is crucial for practical adoption. Additionally, approximate multipliers may interact with other components or modules within the system, requiring careful analysis of the overall system behavior and compatibility with existing computational models.

IV. APPLICATIONS

- Image and Signal Processing: Approximate Wallace-Tree multipliers find extensive use in image and signal processing applications. Tasks such as image and video compression, filtering, and feature extraction can tolerate a certain level of approximation without significantly degrading the visual or auditory quality. By leveraging approximate multipliers, these applications can achieve faster processing times, reduced memory requirements, and improved energy efficiency.

- Machine Learning and Neural Networks: Approximate computing has gained significant attention in the field of machine learning and neural networks. Training and inference in deep learning models often involve computationally intensive matrix multiplications. By employing approximate Wallace-Tree multipliers, it is possible to accelerate the computations while maintaining acceptable accuracy levels. Approximate multipliers can be utilized in neural network layers, such as fully connected layers and convolutional layers, leading to faster training and inference times.

- Internet of Things (IoT) Applications: The IoT ecosystem comprises resource-constrained devices that often operate on limited power sources. Approximate Wallace-Tree multipliers can be applied in IoT applications such as sensor data processing, energy-efficient communication protocols, and real-time analytics. By reducing the computational complexity and power consumption of multiplication operations, approximate multipliers enable efficient processing and analysis of data in IoT devices.

- Cryptography and Security Systems: Approximate multipliers have also found applications in cryptographic systems. Encryption and decryption algorithms involve complex mathematical operations, including modular multiplication. Approximate Wallace-Tree multipliers can be used in cryptographic modules to achieve faster execution while maintaining the necessary security levels. Additionally, for certain cryptographic schemes, controlled approximations can be employed to introduce randomness or obfuscation, enhancing the security properties.

- Embedded Systems and Wearable Devices: Approximate Wallace-Tree multipliers are well-suited for resource-constrained embedded systems and wearable devices. These devices often operate on limited battery power and have strict performance constraints. By leveraging approximate computing, the energy consumption can be significantly reduced, allowing for extended battery life. Moreover, the reduced hardware complexity of approximate multipliers enables the integration of complex functionalities in small form factors.

- Scientific Computing and Simulation: Approximate Wallace-Tree multipliers have applications in scientific computing and simulation tasks. Simulations often involve large-scale computations that can benefit from approximate computing techniques to expedite the results. Scientific simulations that rely on iterative algorithms, numerical methods, and mathematical modeling can be accelerated by employing approximate multipliers, thereby reducing the overall time-to-solution.

- Real-Time Digital Signal Processing: Real-time digital signal processing applications, such as audio and video processing, require high computational efficiency. Approximate Wallace-Tree multipliers can be utilized to accelerate the processing of audio signals, video streams, and other real-time data. By optimizing the multipliers for energy efficiency and reduced latency, real-time processing tasks can be performed more efficiently in various domains, including telecommunications, multimedia systems, and audio/video codecs.

V. CONCLUSION

This review paper aims to provide a comprehensive understanding of the design and implementation of approximate Wallace-Tree multipliers for VLSI applications. It explores various approximation techniques, evaluation metrics, design methodologies, and optimization strategies employed to achieve improved performance and energy efficiency. Furthermore, case studies and applications of approximate multipliers in different domains highlight their practical significance.

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