Design and Implementation of a Seven-Level Switched Capacitor-Based Inverter with Reduced Components and Enhanced Efficiency

Dr K P Parthiban & Mr D Velmurugan
Department of Electrical and Electronics Engineering, VSB College of Engineering Technical Campus, Coimbatore, Tamil Nadu, India.

***Abstract*: -** *A modern plan of a seven-level exchanged capacitor-based inverter plan is proposed with a single DC source, three capacitors, and diminished switches. Lessening the number of switches permits us to decrease exchanging misfortunes compared to customary cascaded MLI. The proposed inverter, which requires no inductor, employments less components than a routine topology. DC levels can be produced by charging and releasing capacitors by suitable exchanging and H-bridges are utilized to accomplish positive and negative cycles at the yield. Separated door control circuitry on the switch is given. The structure of the proposed topology is uncomplicated and can be effortlessly expanded to higher levels of voltage. The proposed topology comes about in decreased establishment range and taken a toll and illustrates the straightforwardness of the control framework. Recreation comes about were gotten to confirm the redress operation of the unused seven-level inverter plan.*

Key Words: Multi Level Inverter (MLI), isolated gate control circuitry, switched-capacitor, switchreduction.

Introduction

The increasing popularity of multi-level inverters (MLIs) for high-power and high-voltage applications is driven by their ability to meet modern power system demands. MLIs offer several advantages, such as utilizing components with lower power ratings, producing high-quality staircase voltage waveforms, and significantly reducing electromagnetic interference (EMI) [9], [10]. These inverters are widely used in grid-connected renewable energy systems, such as solar photovoltaic (PV) systems [7]. However, one of the main challenges of MLIs is their need for numerous components, making them costly, bulky, and prone to failure. As a result, reducing the number of components in MLI topologies is a critical area of research [3].

Several multilevel inverter topologies have been explored in the literature, with common types including diode-clamped, flying capacitor, cascaded H-bridge, full bridge with cascaded transformers, and modified H-bridge MLIs [6]. Among these, the cascaded multilevel inverter (CMI) is particularly popular. Early implementations of CMIs employed low-frequency three-phase transformers and a single DC power source [2]. However, transformer less cascaded multilevel inverters have emerged as promising alternatives for cost-effective and efficient photovoltaic systems [4]. A key challenge with CMI systems is the need for multiple

isolated DC sources, which can complicate their design. Switched-capacitor (SC)-based CMI systems have been developed to address this issue [1], [5].

In recent literature, advancements in traditional three-level MLIs have led to the development of new topologies, such as the single-phase T-type nine-level cascaded H-Bridge (TCHB) MLI, which has been applied in PV systems [8]. In one proposed system, a new switched-capacitor-based seven-level inverter is introduced. This type of inverter converts DC voltage into AC voltage with reduced harmonic distortion, producing seven distinct voltage levels for a smoother output waveform. The design employs a combination of switches and capacitors to generate these voltage levels. Although more complex and expensive compared to other inverters, the improved efficiency and reduced harmonic distortion make seven-level inverters suitable for various high-power industrial applications.

EXISTING SYSTEM

In the current system, a switched-capacitor-based cascaded H-bridge multilevel inverter (SC-CHMI) topology has been implemented, utilizing half-bridge cells and a single DC source to achieve nine-level and eleven-level outputs. The existing inverter configuration requires approximately ten switches and four capacitors to generate a nine-level output, while for an eleven-level output, it employs twelve switches and five capacitors, maintaining its voltage-boosting capability. Figure 1 illustrates the SC-CHMI topology for a nine-level inverter, which utilizes ten switches and four capacitors.

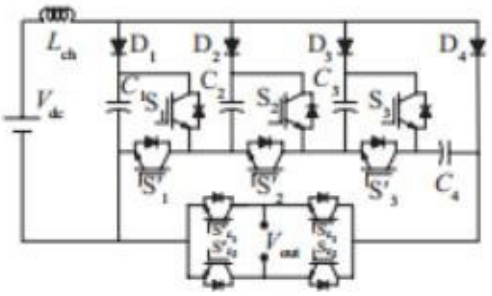

Fig.1 SC-CHMI topology of nine level inverters

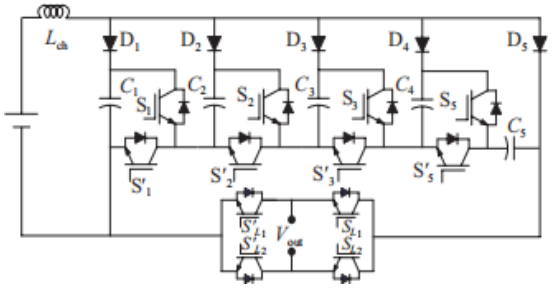

Fig.2 SC-CHMI topology of eleven-level inverter

The existing system utilizes an unfolder bridge along with half-bridge cells for its operation. An eleven-level inverter, which includes four cascaded H-bridge cells, one unfolder bridge, and five capacitors, is depicted in Fig. 2. However, this system faces several challenges, such as higher complexity, increased cost, and the need for more intricate control strategies. To address these limitations, a new switched-capacitor-based seven-level inverter topology has been proposed as an improvement over the current design.

PROPOSED SYSTEM:

The block diagram of the proposed seven-level inverter features a single DC source connected to the multilevel inverter. The switching operations are regulated by control signals generated by a PIC microcontroller, as illustrated in Fig. 3. The microcontroller is powered by a 5V supply, and its output is fed into a driver circuit. The driver circuit, which operates with a 12V supply, then directs control signals to each of the MOSFET switches individually. The inverter's output, approximately 60V AC, is measured across a resistive load.

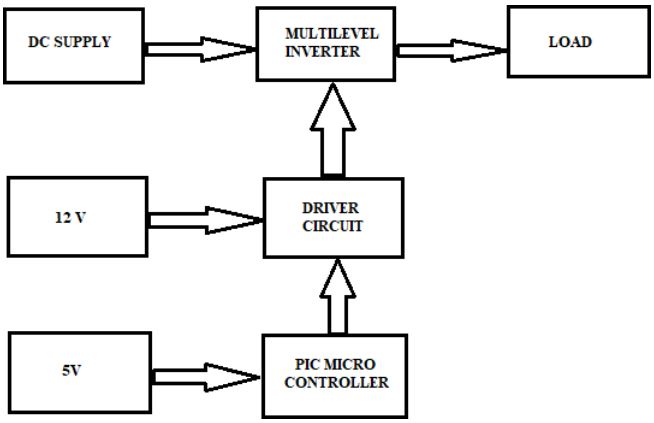

Fig 3. Block Diagram

CIRCUIT DIAGRAM:

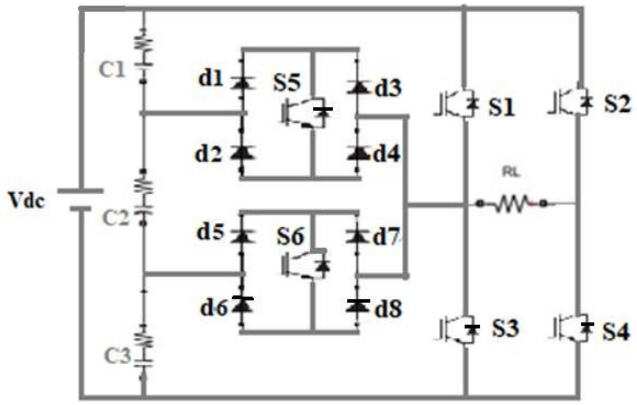

Fig 4. Circuit diagram of inverter

The circuit diagram of the proposed inverter, as shown in Fig. 4, utilizes a single DC supply of approximately 14V. This voltage is supplied to three capacitors that are connected in series. The capacitors function by charging and discharging power, and in this configuration, they act as power sources for the switches. The circuit includes six MOSFET switches. For switches S5 and S6, there are four diodes (d1, d2, d3, d4 for S5, and d5, d6, d7, d8 for S6) connected in parallel. These diodes are arranged to provide the necessary current path and facilitate proper switching operations, while also preventing reverse currents. An H-bridge is incorporated into the design, comprising four switches (S1, S2, S3, and S4), which operate in alternating pairs

(S1 with S4, or S2 with S3) to complete the circuit. A resistive load is connected to the H-bridge to evaluate the output performance.

CIRCUIT OPERATION:

Initially, the source voltage charges all the switched capacitors. Based on the PWM signals, the MOSFET switches are turned ON and OFF to produce the required voltage levels at the output. This operation involves multiple modes. Let's examine the different modes of operation.

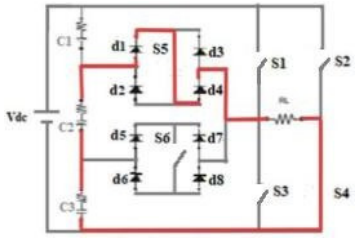

Fig 5(A). Mode I

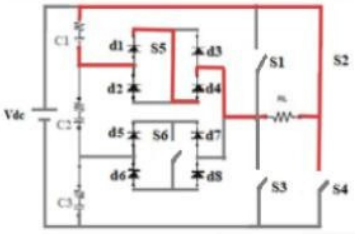

Fig 5(B). Mode II

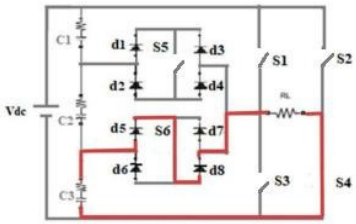

Fig 5(C). Mode III

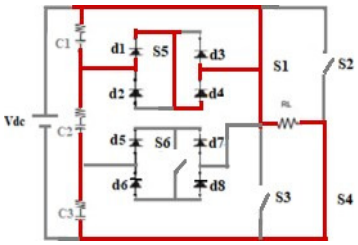

Fig 5(d). Mode IV

Mode I:

In Mode I, switches S5 and S2 are closed, but since switches S3 and S4 remain open, no current flows through the circuit, resulting in an open circuit condition. Therefore, the output voltage is 0V. The current flow is depicted in Fig. 5(a).

Mode II:

In this mode, when switches S4 and S6 are closed, the current flows from capacitor C3 through diodes d5 and d8 to the load, and the circuit completes at the negative terminal of C3. The current path is C3 → d5 → S6 → d8 → RL → S4 → C3, as shown in Fig. 5(b).

Mode III:

When switches S5 and S4 are closed, the current flows from capacitor C2 through diodes d1 and d4 to the load, completing the circuit through the negative terminal of C3. The current path follows C2 → d1 → S5 → d4 → RL → S4 → C3. The remaining switches, S1, S2, S3, and S6, remain open. The flow of current is shown in Fig. 5(c).

Mode IV:

In this mode, switches S5, S1, and S4 are closed. The current flows from capacitors C1, C2, and C3, energizing the load from positive to negative. There are two distinct loops in this mode:

1. C1 → S1 → RL → S4 → C3
2. C2 → d1 → S5 → d4 → RL → S4 → C3

The current flow through these loops is highlighted in Fig. 5(d). This circuit's operation allows for multiple modes, enabling the generation of seven distinct output levels.

Simulation:

Simulation is a software-based method used to predict a system's behavior. The simulation for this project involves a 14V DC supply and three capacitors, with the connections displayed in Fig. 6.

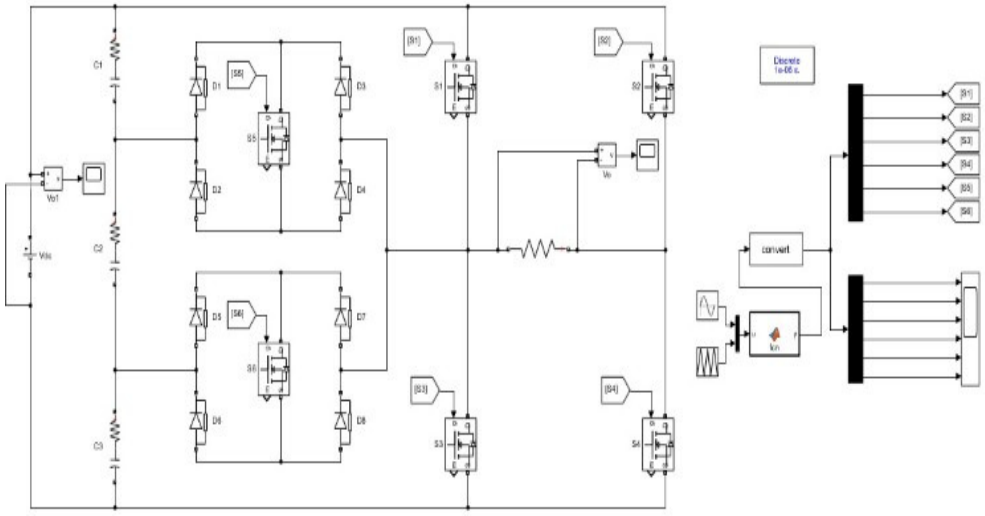

Fig 6. Simulation Diagram

The circuit consists of six switches, eight diodes, and a resistive load. A MATLAB function is programmed with two inputs: a sine wave and a repeating sequence. This function produces a single output, which is fed into a data type conversion block. The output from this block is then supplied as input to two demultiplexers, which are responsible for controlling the switching operations. The demultiplexers are connected to a scope, allowing the observation of the output voltage across each switch, as shown in Fig. 7.

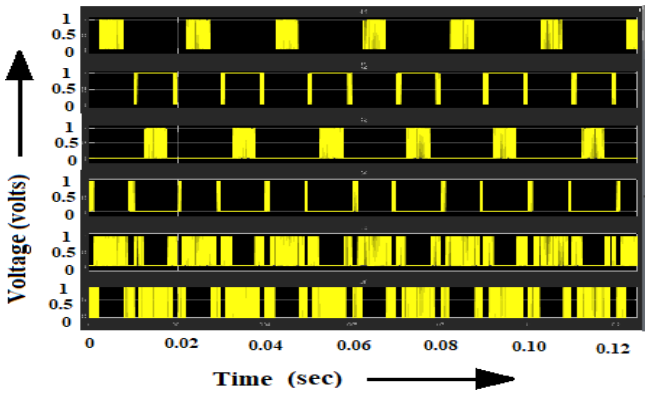

Fig 7. The output waveform of each switch

A seven-level output voltage waveform is produced across the resistive load (RL), which is illustrated in Fig. 8, where the voltage (in volts) is plotted against time (in seconds).

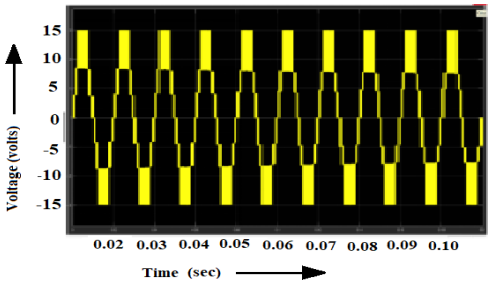

Fig 8. Output Voltage Waveform

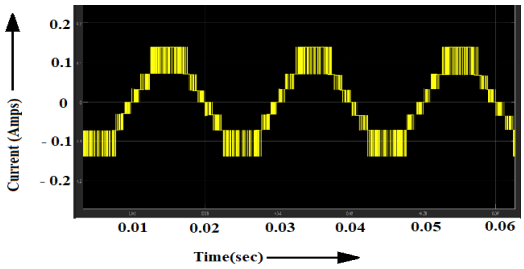

Fig 9. Output Current Waveform

Similarly, a seven-level output current waveform is generated in series with the resistive load, as shown in Fig. 9, where the current (in amps) is plotted against time (in seconds). These simulation results provide insights into the model's performance and help analyze its behavior as conditions change over time.

Hardware Snapshot

Fig.10. Hardware diagram

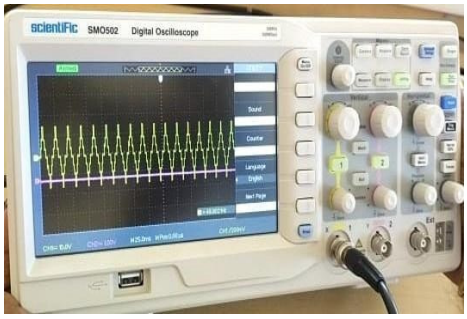

Fig.11.Output waveform

The alternating current is rectified and used as the DC supply for the prototype. The three capacitors then provide power to the MOSFET switches. An additional 12V supply is used to operate the switches via a driver circuit. The switches are controlled by signals from a microcontroller, which is programmed as shown in Fig. 10. With this switched capacitor operation, a seven-level inverter output is achieved. A resistive load is connected to observe the voltage waveform across it, and a seven-level output can be monitored using a digital storage oscilloscope (DSO) connected to the resistive load, as illustrated in Fig. 11. Additionally, a 2W bulb is connected as another load.

A multi-port is integrated at the input side, allowing for various types of DC supplies, such as renewable energy sources like solar power.

Conclusion

This project presents a seven-level inverter design with a reduced number of switches and supply sources. The system uses only one supply and six MOSFET switches to generate a seven-level output. Switched capacitors are used instead of multiple power sources. By adjusting the PWM signals, a seven-level output is obtained. The concept was validated using MATLAB simulation and a low-power prototype model.

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